C9C

Docket Number: INFNP117US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of:

Inventor(s):	Leon Chia-Liang Lin	Art Unit:	2616
Patent No.:	7,106,753	Examiner:	Warner Wong
Issue Date:	September 12, 2006	Serial No.:	10/057,501

Title: INTERPOLATED TIMING RECOVERY SYSTEM FOR COMMUNICATION TRANSCEIVERS

Certificate
OCT 23 2006
of Correction

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 2231301450

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR PTO'S MISTAKE

Sir:

1. It is noted that an error appears in this patent of a clerical, typographical; and minor nature or character as more fully described below , in Appendix A, and occurred in good faith and correction thereof does not involve such changes in the patent as would constitute new matter or would require reexamination and a certificate of correction is requested.

2. Attached hereto is form PTO-1050 suitable for printing. Also attached are documents which substantiate that the error incurred is attributed solely to the USPTO.

3. The exact page and line number where the error (or lack of error, in the event of a mistake by the Patent Office) occurs in the application file are:

Column 16, line 53

4. **No fee is believed to be necessary**.

However, if the error is found to be that of the Applicant's, please deduct the fee as required by 37 CFR 1.20(a), and please charge Deposit Account No. 50-1733 the sum of $100.00.

5. Attached hereto is Appendix A which sets for the reasons **Applicants believe that no fee is due.**

6. Please send the Certificate to

Name: Thomas G. Eschweiler

Address Eschweiler & Associates, LLC
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Date: October 16, 2006

Thomas G. Eschweiler
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CERTIFICATE OF MAILING (37 CFR 1.8(a))

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: October 16, 2006

Christine Gillroy

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.: 7,106,753

Issued: September 12, 2006

Patentee: Leon Chia-Liang Lin

Title: INTERPOLATED TIMING RECOVERY SYSTEM FOR COMMUNICATION TRANSCEIVERS

APPENDIX A

The above-captioned Letters Patent contains a typographical error made by the Patent Office. Specifically, the error is as follows:

Column 16, line 53: Please replace the data sequence "13x,a" to --T3x,a--.

This error is typographical in nature and was committed by the Patent Office. Furthermore, correction of this error does not require such changes in the patent as would constitute new matter or would require re-examination. Therefore, a certificate of correction is respectfully requested.

For this reason, it is believed that the revisions required by the Certificate of Correction is **due to an error made by the Patent Office**. As such, the Patentee is entitled to a Certificate of Correction under 37 C.F.R. §1.322, **and no fee is believed due.**

PTO/SB/44 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,106,753

APPLICATION NO.: 10/057,501

ISSUE DATE : September 12, 2006

INVENTOR(S) : Leon Chia-Liang Lin

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 16, line 53: Please replace the data sequence "13x,a" to --T3x,a--.

MAILING ADDRESS OF SENDER (Please do not use customer number below):
Eschweiler & Associates LLC
National City Bank Building
629 Euclid Avenue, Suite 1000
Cleveland, Ohio 44114

10. The transceiver in accordance with claim 9 wherein the first means adjusts the second frequency of the third clock signal and the time-average frequency of the second clock signal in response to the seventh data sequence.

11. The transceiver in occurrence with claim 9 wherein the ninth means comprises a first finite impulse response (FIR) filter producing each of the elements of the second data sequence as a weighted sum of a plurality of the elements of the sixth data sequence with weighting controlled by values of first coefficients applied as input to the first filter, and

wherein the tenth means comprises a second FIR filter producing each of the elements of the fifth data sequence as a weighted sum of a plurality of the elements of the seventh data sequence with weighting controlled by values of second coefficients applied as input to the second filter.

12. The transceiver in accordance with claim 11 wherein the first means adjusts the values of the first and second coefficients in response to the edges of the first clock signal.

13. The transceiver in accordance with claim 12 wherein the values to which the first means adjusts the first and second coefficients are functions of values of elements of the seventh data sequence.

14. The transceiver in accordance with claim 13 wherein the first means comprises:

a slicer (111) for rounding values of the elements of the seventh data sequence to produce corresponding elements of an eighth data sequence,

means (110-105) for generating a phase data value (D7) that is a function of a difference between the corresponding elements of the seventh and eighth data sequences,

an accumulator (105) for accumulating the phase data value to produce a sequence of control data values (τ) and for asserting a mask signal whenever the control data value reaches a predetermined limit;

means (106) responsive to the mask signal for masking the edges of the first clock signal when the mask signal is asserted to produce the second clock signal;

means (100) for generating the third clock signal in response to the first clock signal and the control data value such that the second frequency is a function of the control data value, and

means (84 and 96) for producing the first and second coefficients as functions of values of elements of the control data sequence.

15. The transceiver in accordance with claim 14 wherein the means (100) for generating the third clock signal comprises:

means (101) responsive to the first clock signal for generating a plurality of reference clock signals, each having edges occurring with said first frequency but with each reference clock signal having a unique phase; and

means (103,104) for generating edges of the third clock signal in response to the edges of the reference clock signals selected in accordance with the values of the control data sequence.

16. A data communication method comprising the steps of:

a. receiving elements of a first data sequence (Tx,a) at a first rate controlled by a first clock signal (CLK3L) and processing the first data sequence to generate elements of a second data sequence (T3x,a) at a second rate controlled by a second clock signal (CLK1L), wherein the second rate is higher than the first rate and wherein the second data sequence is an encoded version of the first data sequence;

b. converting the second data sequence into an analog signal (A1) and transmitting the analog signal via a communication channel;

c. receiving and processing the analog signal transmitted by the communication channel to generate elements of a third data sequence (R3x,a) at a third rate controlled by a third clock signal (CLK1R);

d. processing the third data sequence (R3x,a) to generate elements of a fourth data sequence (Rx,a) at a fourth rate controlled by a fourth clock signal (CLK3R), wherein the fourth rate is lower than the third rate, and wherein the first and fourth data sequences are substantially similar and forwarding the fourth data sequence at the fourth rate;

e. deriving the first clock signal from the second clock signal;

f. deriving the fourth clock signal from the third clock signal;

g. periodically adjusting first coefficient values supplied as input to a first finite impulse response (FIR) filter in response to the second clock signal,

h. periodically adjusting second coefficient values supplied as input to a second finite impulse response filter in response to the third clock signal; and

wherein step e comprises the substeps of:

e1. generating a plurality of reference clock signals, each having edges occurring with a frequency matching the frequency of the second clock signal but with a unique phase; and

e2. generating edges of the second clock signal in response to edges of the reference clock signals selected such that the resulting first clock signal has a time-average frequency substantially matching a frequency of the fourth clock signal.

17. The method in accordance with claim 16 wherein step a comprises the substeps of:

a1. masking portions of the second clock signal (CLK1L) to produce a fifth clock signal (CLK1L), and

a2. shifting elements of the first data sequence (Tx,a) into a first-in, first-out (FIFO) buffer at the first rate controlled by the first clock signal (CLK3L);

a3. shifting elements of the first data sequence out of the first FIFO buffer at a fifth rate controlled by the fifth clock signal (CLK2L);

a4. processing the first data sequence as it is shifted out of the first FIFO buffer to generate the elements of the second data sequence (13x,a) at the second rate controlled by the second clock signal (CLK1L), and

wherein step d comprises the substeps of:

d1. masking portions of the third clock signal (CLK1R) to produce a sixth clock signal (CLK2R),

d2. processing the third data sequence (R3,xa) to generate elements of the fourth data sequence (R1,a) at a sixth rate controlled by the sixth clock signal (CLK2R),

d3. shifting elements of the fourth data sequence into a second FIFO buffer at a sixth rate controlled by the sixth clock signal (CLK2R), and

d4. shifting elements of the fourth data sequence out of the second FIFO buffer and forwarding them at the fourth rate controlled by the fourth clock signal (CLK3R).

a1. masking portions of the second clock signal (CLK1L) to produce a fifth clock signal (CLK1L), and

a2. shifting elements of the first data sequence (Tx,a) into a first-in, first-out (FIFO) buffer at the first rate controlled by the first clock signal (CLK3L);

a3. shifting elements of the first data sequence out of the first FIFO buffer at a fifth rate controlled by the fifth clock signal (CLK2L);

a4. processing the first data sequence as it is shifted out of the first FIFO buffer to generate the elements of the second data sequence (T3x,a) at the second rate controlled by the second clock signal (CLK1L), and

wherein step d comprises the substeps of:

d1. masking portions of the third clock signal (CLK1R) to produce a sixth clock signal (CLK2R),

d2. processing the third data sequence (R3,xa) to generate elements of the fourth data sequence (R1,a) at a sixth rate controlled by the sixth clock signal (CLK2R),

d3. shifting elements of the fourth data sequence into a second FIFO buffer at a sixth rate controlled by the sixth clock signal (CLK2R), and

d4. shifting elements of the fourth data sequence out of the second FIFO buffer and forwarding them at the fourth rate controlled by the fourth clock signal (CLK3R).

25. (Previously Presented) The method in accordance with claim 24 wherein substep a4 comprises the substeps of:

a41. trellis code modulation encoding the first data sequence as it is shifted out of the FIFO buffer to generate elements of a fifth data sequence (T2x,a), and

a42. applying the fifth data sequence as input to a first filter which interpolates elements of the fifth data sequence (T2x,a) to produce elements of the second data sequence (T3x,a) at said second rate, and

wherein substep d2 comprises the substeps of:

d21. applying the third data sequence as input to a second filter which